
Image Processor Peripheral LSI

Description

The ZEN1752F is Image Processor Peripheral LSI, which contains GPIO,I2C master,SPI,PWM outputs,infrared remote control inputs,UART and pulse counters.

Each function block can go to standby mode independently,so that the power consumption can be reduced.

Indirect addressing to internal registers is built in for the small package.

It has independent two clock inputs. The clock of each function block is selectable from them.

1.Features

CPU Interface : 8bit(Indirect addressing)

GPIO : Max36pin(20pin: Dual purpose)

They can be programmed to input or output .

Io=±16mA(4pin), Io=±4mA(32pin)

Each function block can go to standby mode independently.

I2C Bus Master : Max:3ch(The pins are shared by SPI)

SPI : Max:3ch(The pins are shared by I2C)(Ch.0 can be connected to initialization EEPROM.)

PWM : 3ch

Infrared remote control input : 3ch

UART(16550 compatible) : 4ch

Pulse counter : Max:8ch(Up input)(4ch:Phase-shifted inputs)

Independent two clock inputs : Max:50MHz

Power supply voltage : Single 3.3V±0.3V

Input : 5V tolerant

Package : TQFP80(12mm × 12mm , Pitch:0.5mm)

2. Block Diagram

