

ZEN7201AF DATA SHEET

ZENiC Inc.

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◆Description

ZEN7201AF is a PCI bus interface IC designed specific for PCI, CompactPCI target board applications. It features various ideal functions controlled by Mode Register settings.

The maximum 16Mbytes memory space and 64Kbytes I/O space are available on the local bus side. The width of the local address bus is 24 bit. The I/O (memory) address space can be larger than the size assigned by the PCI host controller during the Configuration cycle because ZEN7201AF has the special function for address remapping.

The width of the local data bus is 16bit. Both of the byte and word accesses are available. ZEN7201AF uses the local signals LADR[0]/BLE# and BHE# to indicate the valid byte lane.

ZEN7201AF outputs the local control signals such as IOW#, IOR#, MEW# and MER# synchronized with the local clock. And the timing of the local access is configurable. The Mode registers and the local signal WAIT# control the local read/write timing.

The local interrupt signal can be forwarded to the PCI interrupt line INTA#.

Some parts of the PCI Configuration Registers and the Mode Registers are configurable by an outer EEPROM. You can also read or write it via ZEN7201AF.

The access procedure on the local bus is so simple that you can convert old ISA boards to new PCI products with a minimum modification.

1. Features

- 32bit and 33MHz operation on PCI
- Maximum local clock frequency is 33MHz
- Local memory space 16Mbyte and I/O space 64Kbyte
- The local control signals synchronized with the local clock
- 24bit local address bus and 8/16bit local data bus
- Built-in address decoder for local I/O Access
- 64byte mode register
- Access waiting(by using WAIT#)
- Programmable interrupt circuit
- Built-in EEPROM control circuit
- Hot Swap registers for CompactPCI
- 5V single power supply
- CMOS
- QFP144 pin package

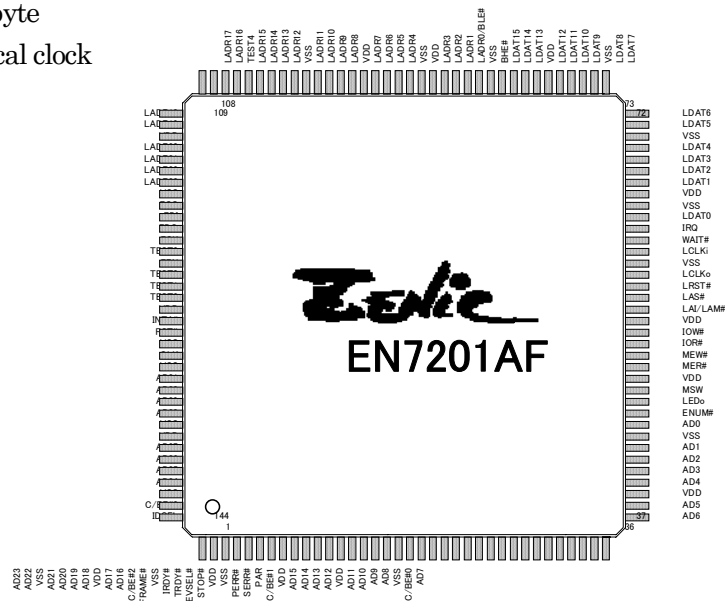


Fig.1 Pin Assign(Top View)

2. System Architecture

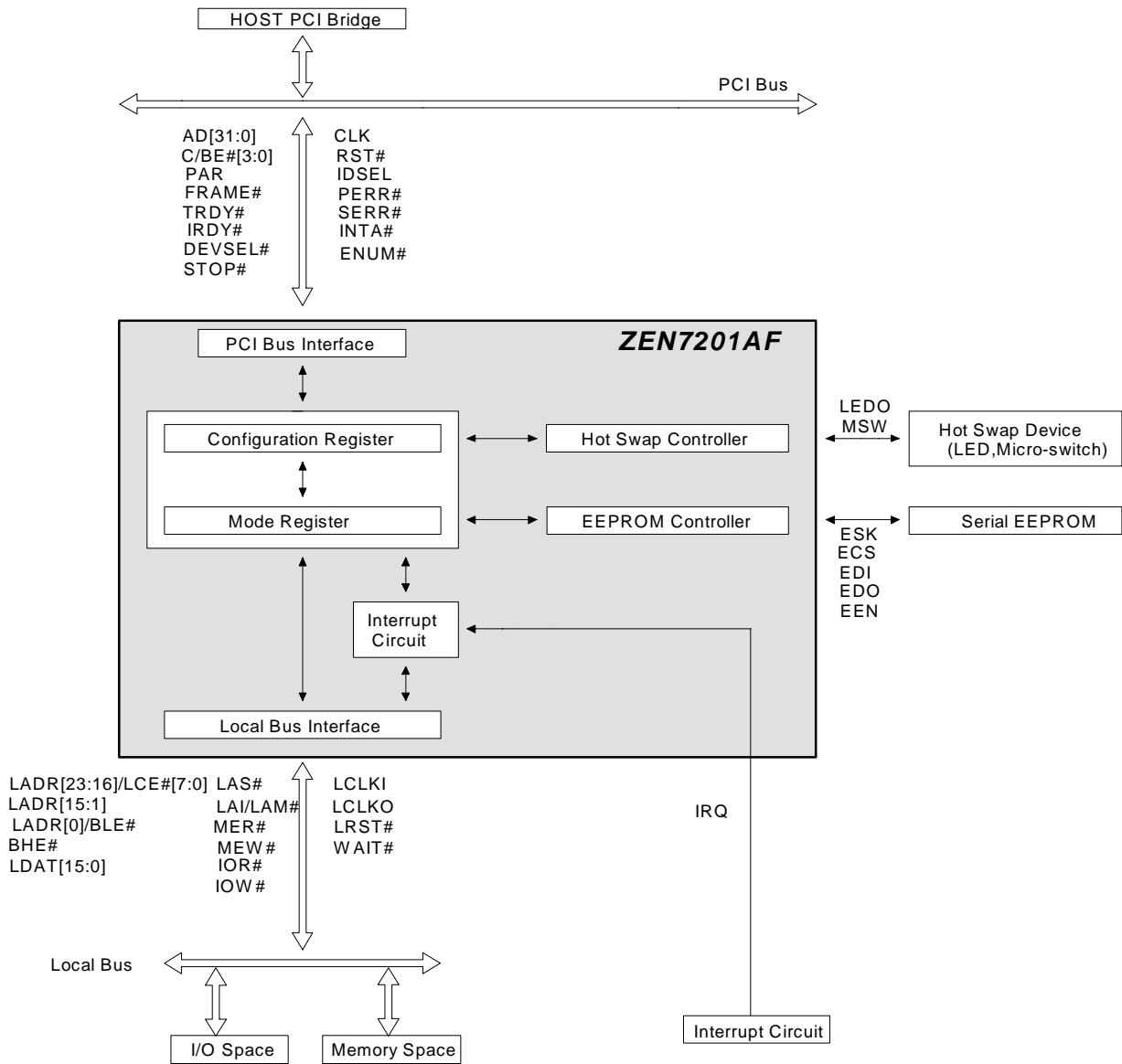


Fig.2 System Block Chart

3. Pin Description

The tables 1-5 describe the pins of ZEN7201AF. '#' on the tables stands for a negative signal.

3.1. PCI Bus Interface Pin Description

Table 1. PCI Bus Interface Pin

No.	Symbol	Name	I/O	Function
130	CLK	PCI Clock	IN	CLK provides timing for all transactions on PCI.
128	RST#	PCI Reset	IN	RST# is used to bring PCI-specific registers, sequencers, and signals to a consistent state.
132-135 138-141 1 2 4-7 9 10 25-28 30-33 36-38 40-43 45	AD[31:0]	Address/Data	I/O	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more dataphase.
143 11 23 35	C/BE#[3:0]	Bus Command /Byte Enable	IN	These are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE#[3:0] define the bus command. During the data phase, C/BE#[3:0] are used as Byte Enables.
22	PAR	Parity	I/O	PAR is even parity across AD[31:0] and C/BE#[3:0]. Parity generation is required by all PCI agents.
12	FRAME#	Cycle Frame	IN	FRAME# is asserted to indicate a bus transaction is beginning.
14	IRDY#	Initiator Ready	IN	IRDY# indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
15	TRDY#	Target Ready	OUT	TRDY# indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
16	DEVSEL#	Device Select	OUT	DEVSEL# indicates the driving device has decoded its address as the target of the current access.

No.	Symbol	Name	I/O	Function
17	STOP#	Bus Stop	OUT	Stop indicates the current target is requesting the master to stop the current transaction.
144	IDSEL	Initialization Device Select	IN	IDSEL is used as a chip select during configuration read and write transactions.
20	PERR#	Parity Error	OUT	PERR# is only for the reporting of data parity errors during all PCI transactions except a Special Cycle.
21	SERR#	System Error	OUT	SERR# is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
127	INTA#	Interrupt	OUT	SERR# is for reporting address parity errors, data parity errors

3.2. Hot Swap Control Pin Description

Table 2. Hot Swap Control Pin

No.	Symbol	Name	I/O	Function
46	ENUM#	Enumeration	OUT	ENUM# is provided to notify the system host that either a board has been freshly inserted or is about to be extracted.
47	LEDO#	LED On	OUT	LEDO# is used to drive the LED which indicates a state for orderly extraction of the board.
48	MSW	Microswitch On/Off	IN	MSW is connected to the microswitch of the eject handle. ZEN7201AF detects the board is about to be inserted or ejected.

3.3. EEPROM Control Pin Description

Table 3. EEPROM Control Pin

No.	Symbol	Name	I/O	Function
120	ESK	EEPROM Clock	OUT	ESK is the clock for EEPROM.
117	ECS	EEPROM Chip Select	OUT	ECS is the chip select for EEPROM.
118	EDI	EEPROM Data IN	IN	EDI reads data from EEPROM.
119	EDO	EEPROM Data OUT	OUT	EDO writes data to EEPROM.
122	EEN	EEPROM Enable	IN	EEN enables EEPROM.

3.4. Local Bus Interface Signal

Table 4. Local Bus Interface Pin

No.	Symbol	Name	I/O	Function
56	LAS#	Local Access Start	OUT	LAS# indicates beginning of local access cycle.
55	LAI/LAM#	Local Access I/O/Memory	OUT	LAI/LAM# is asserted "0" for memory access and "1" for I/O access.
60	LCLKI	Local Clock Input	IN	LCLKI is the local clock input.
58	LCLKO	Local Clock Output	OUT	LCLKO is the local clock output. The frequency is half of PCI clock. This pin may be connected to LCLKI.
57	LRST#	Local Reset	OUT	LRST# resets the local devices.
83-81 79-76 74-71 69-66 63	LDAT[15:0]	Local Data	I/O	LDAT[15:0] are the local data bus.
115-112 110-107	LADR[23:16] /LCE#[7:0]	Local Address /Local Chip Enable	OUT	For memory access, LADR[23:16]/ LCE#[7:0] are the local address bus. And for I/O access, these are the chip enable pins.
105-102 100-97 95-92 89-87	LADR[15:1]	Local Address	OUT	LADR[15:1] are the local address bus.
86	LADR[0] /BLE#	Local Address /Byte Low Enable	OUT	For 8 bit mode, this pin is the 0th bit of address bus. For 16 bit mode, this pin indicates the lower byte lane(LDAT[7:0]) is active.
84	BHE#	Byte High Enable	OUT	For 16 bit mode, this pin indicates the upper byte lane(LDAT[15:8]) is active.
50	MER#	Memory Read	OUT	MER# is asserted low for memory read.
51	MEW#	Memory Write	OUT	MEW# is asserted low for memory write.
52	IOR#	I/O Read	OUT	IOR# is asserted low for I/O read.
53	IOW#	I/O Write	OUT	IOW# is asserted low for I/O read.
61	WAIT#	Access Wait	IN	WAIT# can be asserted to insert some wait states. It causes the strobe signal(MER#, MEW#, IOR# or IOW) is extended.
62	IRQ	Interrupt Request	IN	IRQ is the input for local interrupt request.

3.5. Power, Ground and Testing Pin Description

Table 5. Power, Ground and Testing Pin

No.	Symbol	Name	I/O	Function
121 106 125-123	TEST#[4:0]	Test	IN	TEST#[4:0] are used to test only. NORMALLY, THESE PINS MUST BE CONNECTED TO VDD.
8 18 24 29 39 49 54 65 80 90 96 111 126 137	VDD	Power	-	Power supply pins (+5V).
3 13 19 34 44 59 64 70 75 85 91 101 116 129 131 136 142	VSS	Ground	-	Ground pins.

4. Functions

4.1. PCI Bus Access

4.1.1. PCI Bus Access

The basic functions on PCI bus depend on PCI Local Bus Specification.

Table 6 shows which bus command is supported (o => supported, x => not supported).

Table 6. Bus Command

Cycle	Command	Bus Command				support
		C/BE#3	C/BE#2	C/BE#1	C/BE#0	
I/O Cycle	I/O Read	0	0	1	0	o
	I/O Write	0	0	1	1	o
Memory Cycle	Memory Read	0	1	1	0	o
	Memory Read Line (*1)	1	1	1	0	o
	Memory Read Multiple (*1)	1	1	0	0	o
	Memory Write	0	1	1	1	o
	Memory Write & Invalidate(*2)	1	1	1	1	o
CFG(*3) Cycle	Configuration Read	1	0	1	0	o
	Configuration Write	1	0	1	1	o
Interrupt Acknowledge		0	0	0	0	x
Special Cycle		0	0	0	1	x
Dual Address Cycle		1	1	0	1	x
Reserved		0	1	0	0	x
		0	1	0	1	x
		1	0	0	0	x
		1	0	0	1	x

*1 Same as Memory Read

*2 Same as Memory Write

*3 CFG=Configuration

If any PCI master chip issues above unsupported commands to ZEN7201AF, DEVSEL# is never asserted, so that master abort will be caused.

4.1.2. Exceptional Transaction

ZEN7201AF acts as following table when the exceptional transaction occurs.

Table 7. Exceptional Transaction

Error	Response
Address Parity Error	1. No response(it results in Master Abort). 2. SERR# is asserted if the bit[8] and bit[6] in command register of configuration registers are "1".
Data Parity Error	1. Responding normally. 2. PERR# is asserted if the bit [8] in command register of configuration registers is "1".
Detecting PERR# asserted	1. Responding normally.
Detecting unsupported bus command	1. No response(it results in Master Abort).
Detecting unsupported BE#[3:0] combinations	1. Generating Target Abort.

4.1.3. Target Initiation Termination

4.1.3.1. Disconnect

ZEN7201AF always terminates the transaction with Disconnect because ZEN7201AF is not capable of doing a burst. When a master tries to do a burst, ZEN7201AF acts as follows:

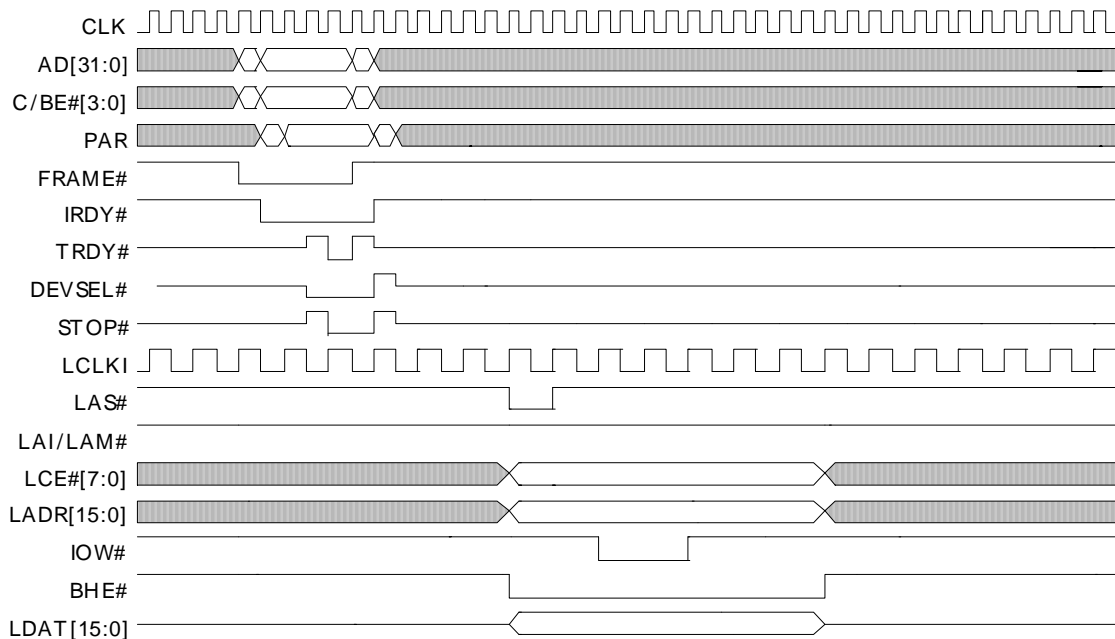

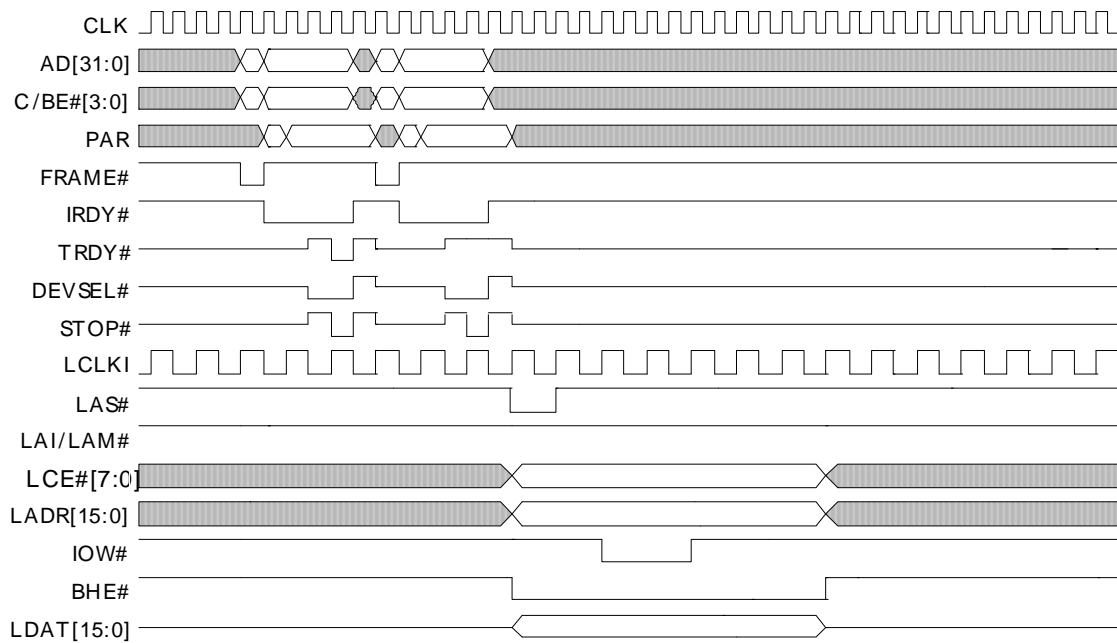


Fig.3 Disconnect Timing

4.1.3.2. Retry

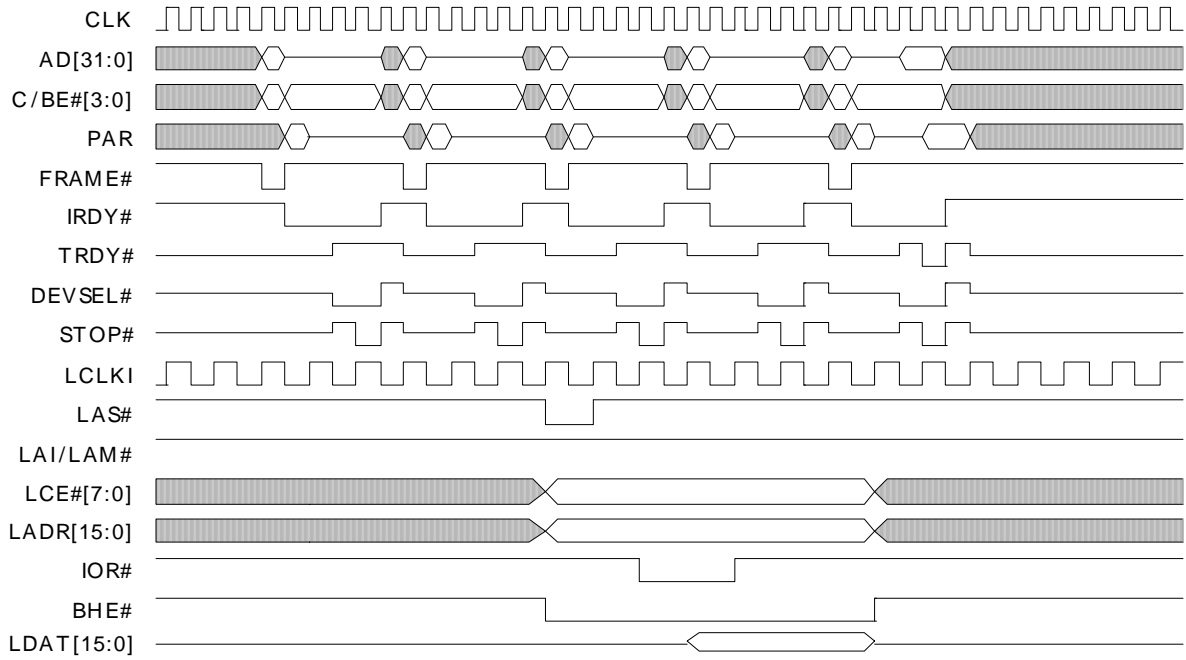
As to read transactions (I/O Read or Memory Read), ZEN7201AF always performs Delayed Transaction. The following timing diagram shows a typical operation  a Delayed Transaction.

And even if the transaction is write operation, ZEN7201AF terminates the transaction with Retry when the local bus is busy.



(a) Write Access

Fig.4 Retry Timing



(b) Read Access

Fig.4 Retry Timing

4.2. Local Bus Access

ZEN7201AF transfers the address from PCI bus to the local bus. The local memory space is 16Mbyte and the local I/O space is 64Kbyte. So ZEN7201AF uses LADR[23:0] for addressing in memory space. In the case of I/O access, LADR[15:0] is used for addressing and LADR[23:16](LCE#[7:0]) can be used as chip enable pins(if the bit 27 of the Timing Control Register is set 1).

The local bus access cycle begins with asserting LAS# "0". And LAI/LAM# indicates whether the cycle is the memory access or the I/O access.

Table 8. Patterns of Local Access

Signal			Timing Control Register Bits[27]	Access	Note
LAS#	LAI/LAM#	LADR[23:16]/LCE#[7:0]			
0	0	LADR[23:16]	X	Memory	
0	1	LCE#[7:0]	1	I/O	I/O Space deviding available
0	1	All "1"	0	I/O	I/O Space deviding unavailable
1	1	-	X	-	

ZEN7201AF supports the following combinations of AD[1:0] and BE#[3:0]. ZEN7201AF is incapable of performing Word or Double Word access with an odd address. ZEN7201AF terminates the transaction with Target Abort when ZEN7201AF detects unsupported combinations of them.

Table 9. Supported combinations of AD[1:0] and BE#[3:0](memory access)

AD[1:0]	C/BE#[3:0]	LADR[0]/BLE#	BHE#	Access		Note
				PCI Bus	Local Bus	
00	0000	0	0	32 bit	16 bit	
		LADR[0]	1	32 bit	8 bit	
10	0011	0	0	16 bit	16 bit	
		LADR[0]	1	16 bit	8 bit	
00	1110	0	1	8 bit	16 bit	Lower byte valid
		LADR[0]	1	8 bit	8 bit	
01	1101	1	0	8 bit	16 bit	Upper byte valid
		LADR[0]	1	8 bit	8 bit	
10	1011	0	1	8 bit	16 bit	Lower byte valid
		LADR[0]	1	8 bit	8 bit	
11	0111	1	0	8 bit	16 bit	Upper byte valid
		LADR[0]	1	8 bit	8 bit	
XX	1111	-	-	-	-	

Table 10. Supported byte lane in I/O Access

AD[1:0]	C/BE#[3:0]	LADR[0]/ BLE#	BHE#	Access		Note
				PCI Bus	Local Bus	
00	0000	0	0	32 bit	16 bit	
		LADR[0]	1	32 bit	8 bit	
	1100	0	0	16 bit	16 bit	
		LADR[0]	1	16 bit	8 bit	
	0011	0	0	16 bit	16 bit	
		LADR[0]	1	16 bit	8 bit	
	1110	0	1	8 bit	16 bit	Lower byte valid
		LADR[0]	1	8 bit	8 bit	
	1101	1	0	8 bit	16 bit	Upper byte valid
		LADR[0]	1	8 bit	8 bit	
	1011	0	1	8 bit	16 bit	Lower byte valid
		LADR[0]	1	8 bit	8 bit	
	0111	1	0	8 bit	16 bit	Upper byte valid
		LADR[0]	1	8 bit	8 bit	
1111		-	-	-	-	

The following timing diagrams illustrate how local bus transactions (memory write access as a sample) are performed. In these sample cases, bit[15:12](memory access address setup),bit[19:16](memory read/write pulse width) and bit[23:20](memory write address hold) of the timing control register are set all "0000".

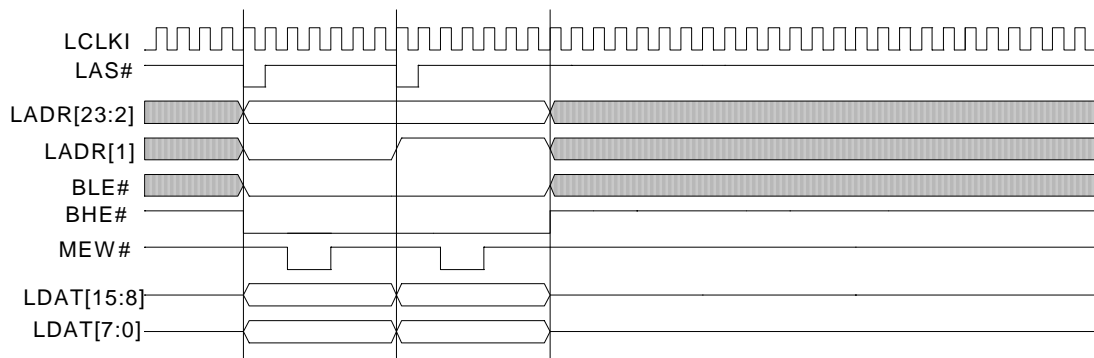


Fig.5 PCI Bus: 4 byte Local Bus: 16 bits

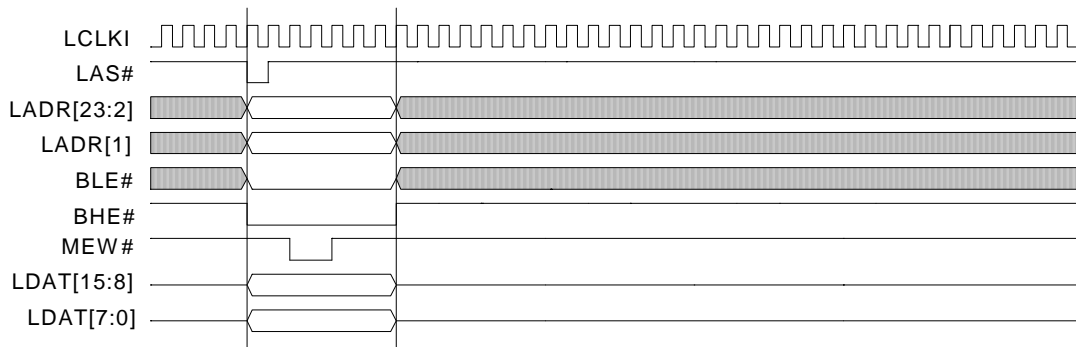


Fig.6 PCI Bus : 2 byte Local Bus : 16 bits

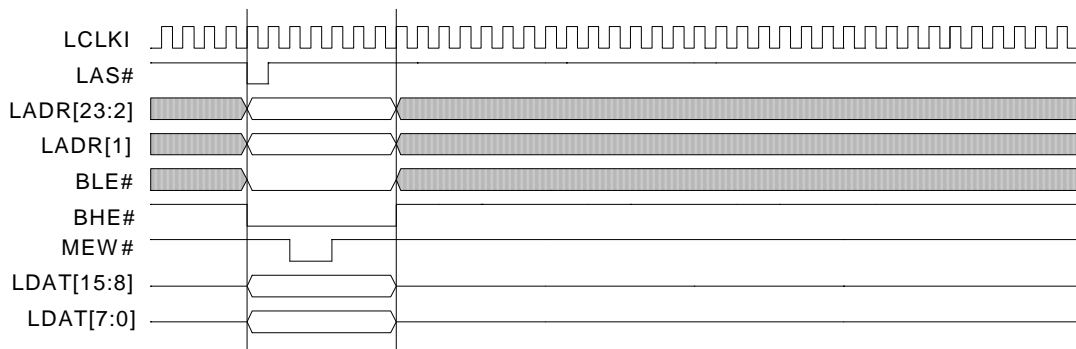


Fig.7 PCI Bus: 1 byte Local Bus: 16 bits (Odd Address)

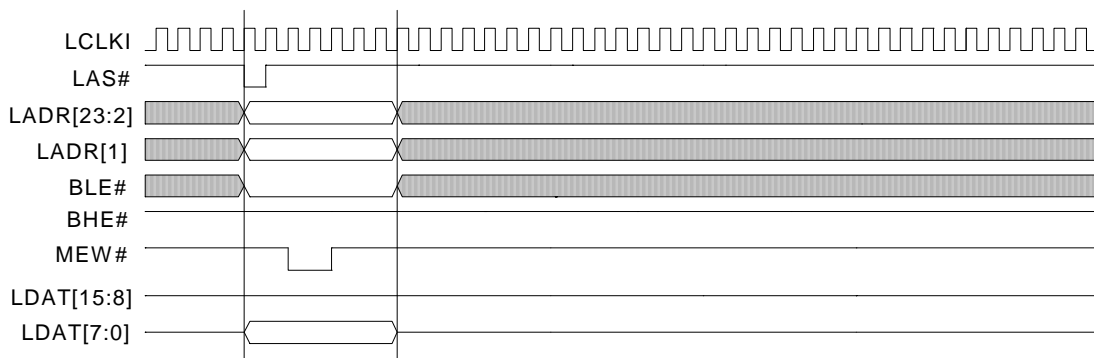


Fig.8 PCI Bus: 1 byte Local Bus: 16 bits (Even Address)

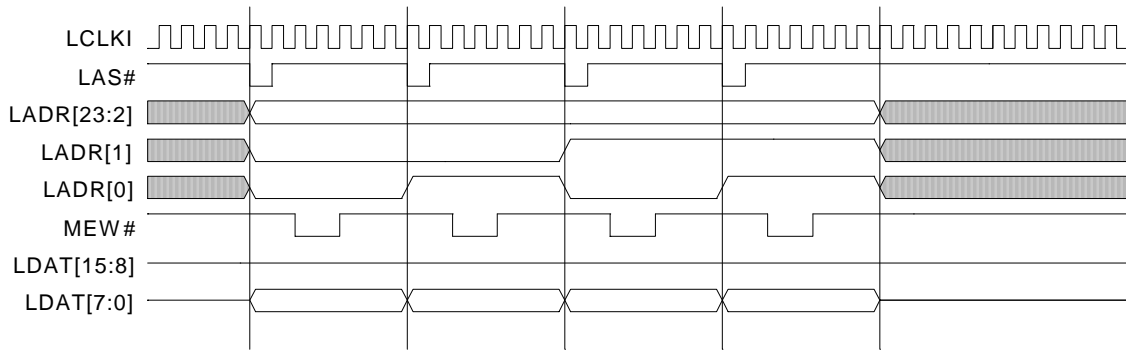


Fig.9 PCI Bus: 4 byte Local Bus: 8 bits

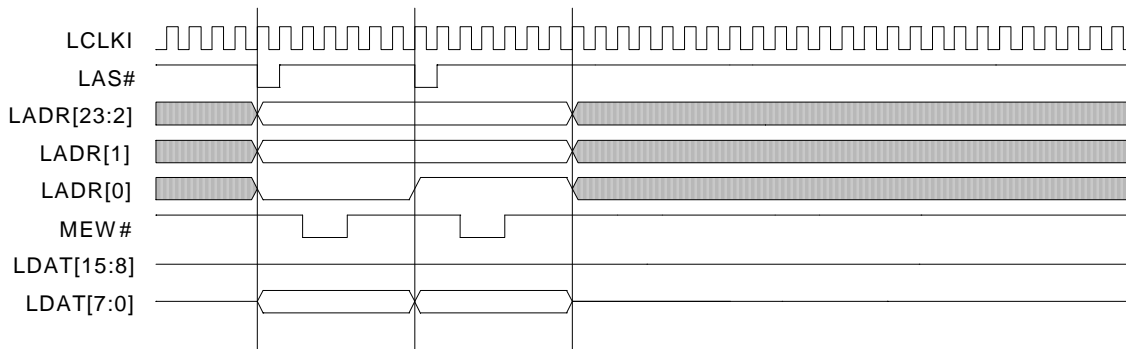


Fig.10 PCI Bus: 2 byte Local Bus: 8 bits

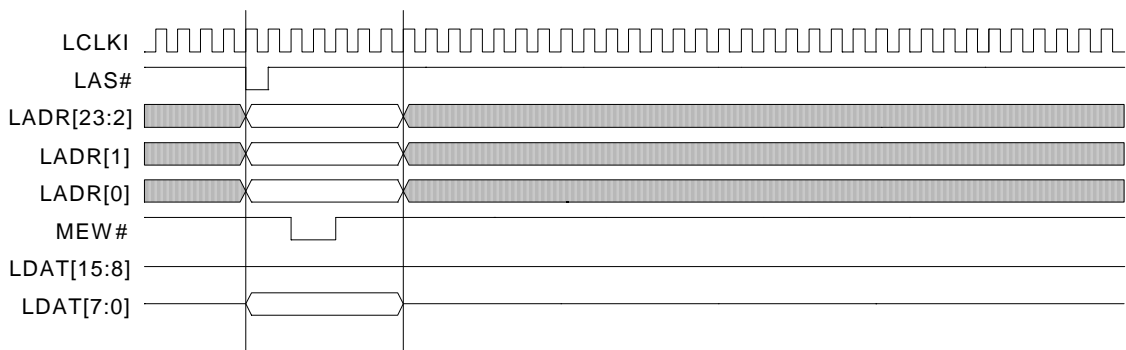


Fig.11 PCI Bus: 1 byte Local Bus: 8 bits

4.2.1. Local I/O Access

The signals for local I/O access are LAS#, LAI/LAM#, IOW#, IOR#, LADR[23:16]/LCE#[7:0], LADR[15:1], LADR[0]/BLE#, BHE#, LDAT[15:0] and WAIT#. The I/O space can be divided into eight parts if bit[27](I/O chip select enable) of the timing control register is set "1". LADR[23:16]/LCE#[7:0] are all deasserted(output "1") when bit[27] is set to "0".

ZEN7201AF has a built-in address decoder for I/O access. Which three bits of LADR[15:8] are to be decoded depends on bit[26:24] of the timing control register.

Table 11. Decoding Table of Local Chip Enable

Value of LADR[n+2,n]			Asserted line of LCE#[7:0]							
X+2	X+1	X	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

Table 12. Decoding Table of I/O Space

I/O Chip Select (bit [26:24])			Local Address LADR [X+2:X]			I/O space separation
26	25	24	X+2	X+1	X	
0	0	0	LADR[8]	LADR[7]	LADR[6]	64byte*8 = 512byte
0	0	1	LADR[9]	LADR[8]	LADR[7]	128byte*8 = 1Kbyte
0	1	0	LADR[10]	LADR[9]	LADR[8]	256byte*8 = 2Kbyte
0	1	1	LADR[11]	LADR[10]	LADR[9]	512byte*8 = 4Kbyte
1	0	0	LADR[12]	LADR[11]	LADR[10]	1Kbyte*8 = 8Kbyte
1	0	1	LADR[13]	LADR[12]	LADR[11]	2Kbyte*8 = 16Kbyte
1	1	0	LADR[14]	LADR[13]	LADR[12]	4Kbyte*8 = 32Kbyte
1	1	1	LADR[15]	LADR[14]	LADR[13]	8Kbyte*8 = 64Kbyte

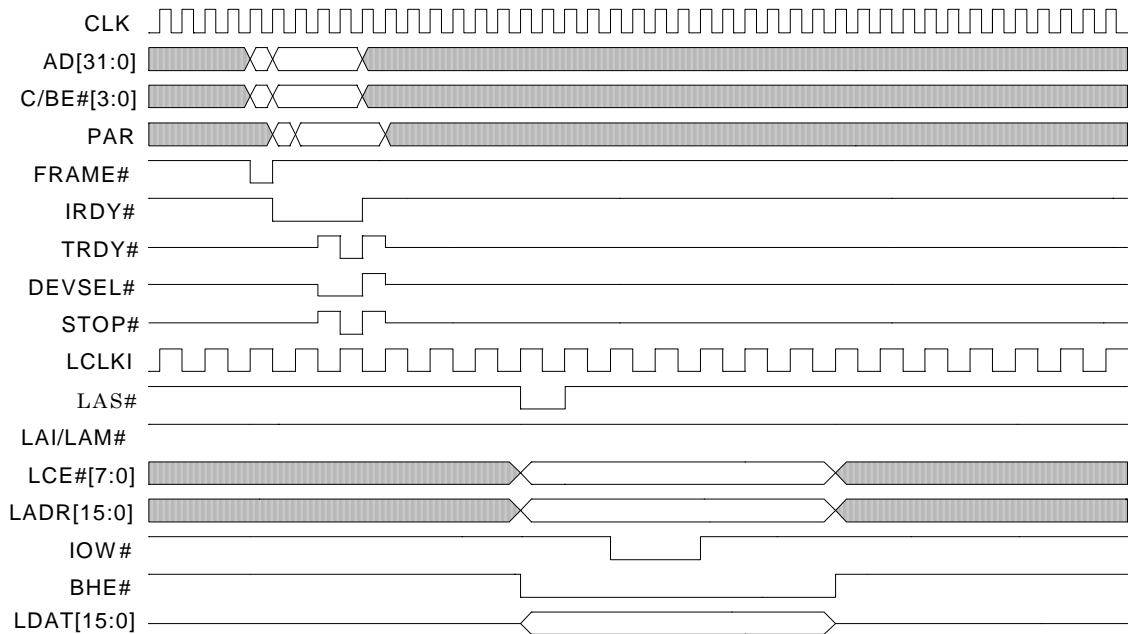


Fig.12 Local I/O Access

4.2.2. Local Memory Access

The signals for Local Memory Access are LAS#, LAI/LAM#, MEW#, MER#, LADR[23:1], LADR[0]/BLE#, BHE#, LDAT[15:0] and WAIT#. LAI/LAM# outputs "0" while Local Memory Access is performed. In local memory space, the built-in address decoder is not available.

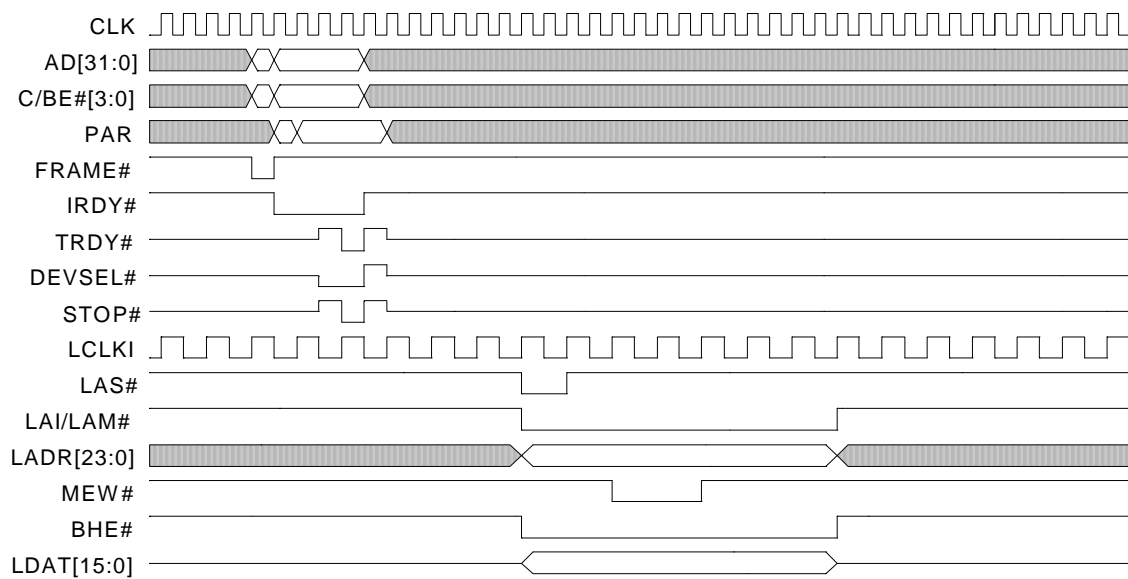
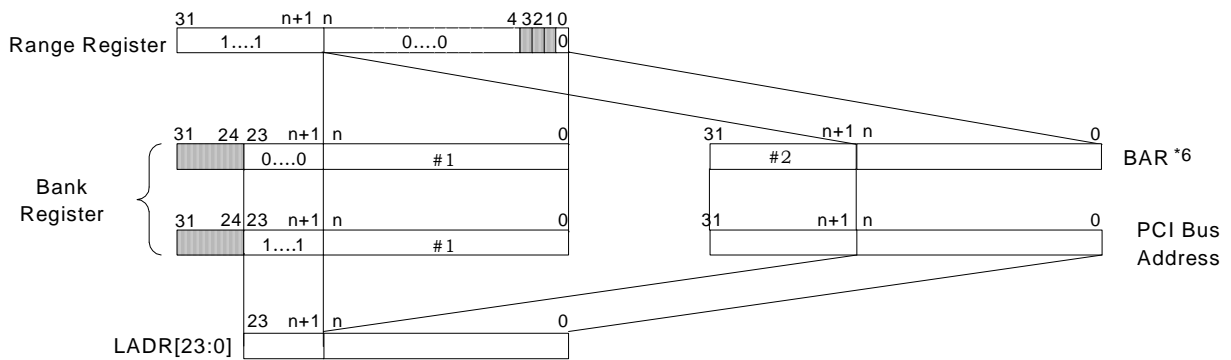


Fig.13 Local Memory Access

4.2.3. Local Bus Addressing

The larger space than the size that a host master assigned in Configuration Cycle is available because ZEN7201AF has Bank Register. For example, the default size of Local Memory Space that ZEN7201AF requires is 1M byte, but with some value(4bit) set to Bank Register[23:20], the Local Memory Space can be expanded to 16M byte. The value of Bank Register[23:20] is assigned to the upper 4bit of the local memory address(LADR[23:0]) and the lower 20bit of the PCI address(AD[19:0]) is passed to the rest 20bit(LADR[19:0]).

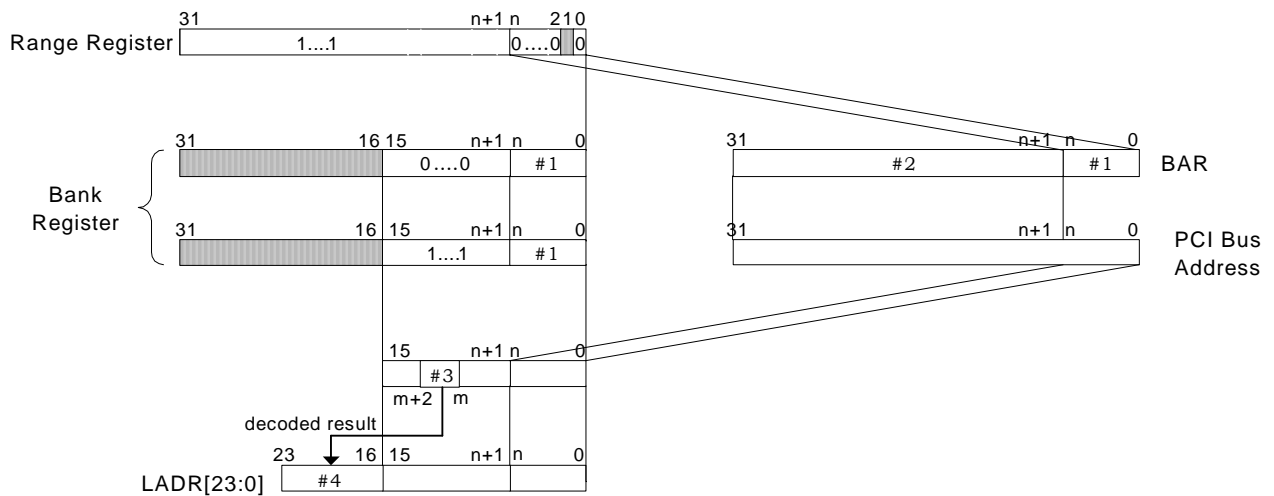
*6 BAR = Base Address Register



#1 : The area required by the Range Register

#2 : The area to be decoded in order to detect the access for ZEN7201AF

Fig.14 Generating Local Address For Memory Space



- #1 : The area required by the Range Register
- #2 : The area to be decoded in order to detect the access for ZEN7201AF
- #3 : The area to be decoded in order to generate a local chip enable.
- #4 : The chip enable signal(LCE#[7:0])

Fig.15 Generating Local Address and Chip Enable For I/O Space

4.2.4. Local Bus Timing Control

Each timing of the address setup, the width of strobe and the address hold can be configured separately. Moreover the width of strobe can be controlled by the input pin WAIT# if the bit[17] of Device Control & Interrupt Control Register is set "1". In this case, WAIT# must be asserted "0" before the strobe signal(IOR#, IOW#, MER# or MEW#) is asserted.

Note: Bit[19:16] and bit[7:4] are ignored when the bit[17] of Device Control & Interrupt Control Register is set "1".

4.2.5. Access Wait

Figure 16 shows a local access with asserting WAIT#(the bit[17] of Device Control & Interrupt Control Register is set "1").

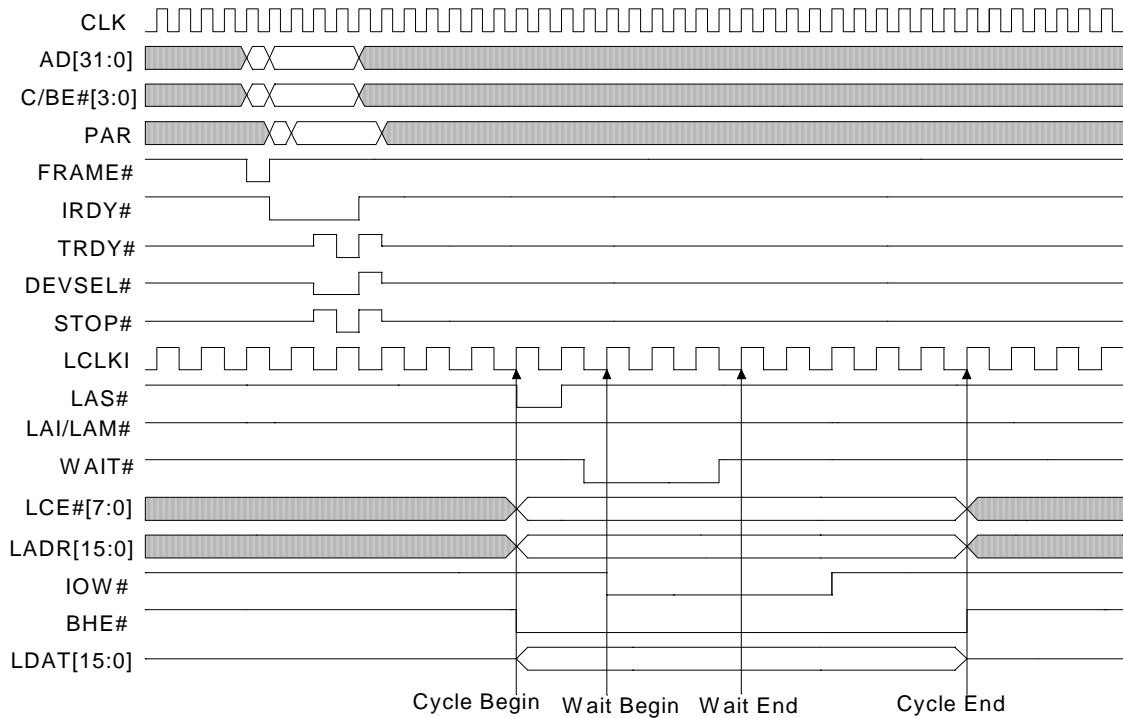


Fig.16 Wait Cycle

4.2.6. Selecting Bus Width(8/16)

ZEN7201AF supports the 8 bit bus and the 16bit bus. Please refer to exsample timings(figure 5 - 11).

4.3. Interruption

The local interrupt signal can be forwarded to the PCI interrupt line INTA# when the bit[0] of Device Control & Interrupt Control Register is set "1".

The condition of accepting the local interrupt signal(IRQ) is configured by the bit[2:1] of Device Control & Interrupt Control Register. The details are as follows:

Figure 13. Condition of accepting Interrupt Request

Bit[2:1] of Device Control & Interrupt Control Register		condition of accepting IRQ
Bit[2]	Bit[1]	
0	0	IRQ: detecting "0" for 2 clocks ("00")
0	1	IRQ: rising edge("01")
1	0	IRQ: falling edge("10")
1	1	IRQ: detecting "1" for 2 clocks("11")

INTA# is deasserted when the bit[4] of Device Control & Interrupt Control Register is set "1".

4.4. EEPROM

The PCI Configuration Registers and the Mode Registers can be initialized by EEPROM(FM93C46). After RST# is deasserted, ZEN7201AF begins to load data from EEPROM to the PCI Configuration Registers and the Mode Registers when the pin EEN is connected to VDD. The clock rate for accessing EEPROM is 1/128 of PCI clock.

If ZEN7201AF detects PCI access during loading data from EEPROM, ZEN7201AF replies with Retry.

In addition to initializing, reading/writing data of each address is available via EEPROM Control Register.

Figure 17 shows the timing diagram of accessing EEPROM for initializing.

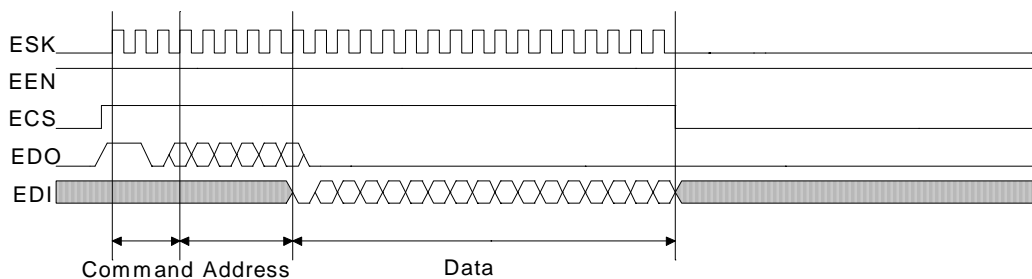


Fig.17 EEPROM Timing Chart

Table 14 .EEPROM Configuration Address

EEPROM Offset Address(h)	Register	Bit	EEPROM Value(h)
00h	Status Register	bit[4]	0410h
01h	Class Code(Programming I/F)/RevisionID	bit[15:0]	0001h
02h	Class Code(Base Class/Sub Class)	bit[15:0]	0680h
03h	Subsystem Vendor ID	bit[15:0]	0000h
04h	Subsystem ID	bit[15:0]	0000h
05h	Interrupt Pin/Interrupt Line	bit[8]	0100h
06h	Range for I/O	bit[15:2]	ffc1h
07h	Reserved	bit[15:0]	0000h
08h	Bank for I/O	bit[15:2]	0000h
09h	Reserved	bit[15:0]	0000h
0ah	Range for Memory(lower word)	bit[15:4]	0000h
0bh	Range for Memory(upper word)	bit[7:0]	fff0h
0ch	Bank for Memory(lower word)	bit[15:4]	0000h
0dh	Bank for Memory(upper word)	bit[7:0]	0000h
0eh	Timing Control(lower word)	bit[15:0]	0000h
0fh	Timing Control(upper word)	bit[11:0]	0000h
10h	Interrupt Control	bit[2:1]	0028h
11h	Device Control	bit[15:8]/[2:1]	0001h

Note: These EEPROM values are just samples. Without EEPROM, these values are set.

4.5. Hot Swap

Hot Swap functions of ZEN7201AF are based on PICMG2.1 Rev1.0. About its details, please refer to Compact PCI Hot Swap Specification.

4.5.1. ENUM#

ENUM# is a signal to notify the system host that either a board has been freshly inserted or is about to be extracted. When ENUM# is asserted, EXT(bit[6]) and INS(bit[7]) of HSCSR show which event happens, extraction or insertion. ENUM# is valid only when bit[17] of HSCSR of PCI Configuration Registers is set "0".

4.5.2. LEDO#

LEDO# controls BlueLED which is to be located on the front of the board. LEDO# is asserted when bit[3] of HSCSR is set "1" or RST# is asserted. This LED indicates that system software has been placed in a state for orderly extraction of the board.

4.5.3. MSW

MSW should be connected to a microswitch which is to be built into an ejector handle. ZEN7201AF detects the insertion of the board when MSW changes from "1" to "0" and the extraction when MSW changes from "0" to "1". if this pin is not used, it should be connected to GND.

5. Registers

At 5.1 - 5.3., the functions of registers are described.

Note: The gray area in following tables is not supported.

5.1. Register Map

Table 15 and 16 show the registers that ZEN7201AF contains.

Table 15.PCI Configuration Register

Offset Address (h)	Bit					
	31	24	23	16 15	8 7	0
00h	Device ID				Vendor ID	
04h	Status Register				Command Register	
08h	Class Code				Revision ID	
0ch	BIST	Header Type		Master Latency Timer	Cash Line Size	
10h	Mode Register Control BAR(for I/O)					
14h	Mode Register Control BAR(for Memory)					
18h	Local Bus Control BAR(for I/O)					
1ch	Local Bus Control BAR(for Memory)					
20h	Reserved					
24h	Reserved					
28h	Card Bus CIS Pointer Register					
2ch	Sub System ID			Sub System Vendor ID		
30h	Expansion ROM BAR					
34h	Reserved				CAP_PTR	
38h	Reserved					
3ch	Max_Lat	Min_Gnt		Interrupt Pin	Interrupt Line	
40h	Reserved	HSCSR		NXT_PTR	CAP_ID	

Table 16. Mode Registers

Offset Address (h)	Bit					
	31	24	23	16	15	8 7 0
00h	Range for I/O					
04h	Bank for I/O					
08h	Reserved					
0ch	Range for Memory					
10h	Bank for Memory					
14h	Reserved					
18h	Timing Control					
1ch	Reserved					
20h	Reserved					
24h	Reserved					
28h	Reserved					
2ch	Reserved					
30h	Reserved				EEPROM Control	
34h	Device Control			Interrupt Control		
38h	Reserved					
3ch	Reserved					

5.2. PCI Configuration Registers

5.2.1. Device ID & Vendor ID

Table 17. Device ID & Vendor ID

Field	Name	Description	Reset Value	R	W	I
31:16	Device ID	ID for ZEN7201AF	01110010 00000001	0	X	X
15:0	Vendor ID	ID for ZENIC	00101110 11000001	0	X	X

5.2.2. Status & Command
Table 18. Status & Command

Field	Name	Description	Reset Value	R	W	I
31	Detected Parity Error	This bit is set when ZEN7201AF detects a parity error.	0	0	0	X
30	Signaled System Error	This bit is set when ZEN7201AF asserts SERR#.	0	0	0	X
29	Received Master Abort	Unsupported	0	0	X	X
28	Received Target Abort	Unsupported	0	0	X	X
27	Signaled Target Abort	This bit is set when a transaction is terminated with Target Abort.	0	0	0	X
26:25	DEVSEL Timing	This bit indicates timing for assertion of DEVSEL#	10	0	X	X
24	Master Data Parity Error Detection	Unsupported	0	0	X	X
23	Fast Back-to-Back Capable	Unsupported	0	0	X	X
22	Reserved	Unsupported	0	0	X	X
21	66MHz Capable	Unsupported	0	0	X	X
20	Capabilities List	This bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h.	1	0	X	0
19:16	Reserved		0000	0	X	X
15:10	Reserved		000000	0	X	X
9	Fast Back-to-Back Enable	Unsupported	0	0	X	X
8	SERR# Enable	When this bit is set "1", SERR# is enabled.	0	0	0	X
7	Stepping Control	Unsupported	0	0	X	X
6	Parity Error Response	When this bit is set "1", PERR# is enabled.	0	0	0	X
5	VGA Palette Snoop	Unsupported	0	0	X	X
4	Memory Write and Invalidate Enable	Unsupported	0	0	X	X
3	Special Cycle	Unsupported	0	0	X	X
2	Bus Master	Unsupported	0	0	X	X
1	Memory Space	When this bit is set "1", this device responds to Memory Space access.	0	0	0	X
0	I/O Space	When this bit is set "1", this device responds to I/O Space access.	0	0	0	X

5.2.3. Class Code & Revision ID
Table 19. Class Code & Revision ID

Field	Name	Description	Reset Value	R	W	I
31:24	Base Class	This 8bit code broadly classifies the type of function.	00000110	O	X	O
23:16	Sub Class	This 8bit code identifies more specifically the function.	10000000	O	X	O
15:8	Programming Interface	This 8bit code identifies a specific register-level programming interface.	00000000	O	X	O
7:0	Revision ID	This 8bit code specifies a device specific revision identifier.	00000001	O	X	O

5.2.4. BIST & Header Type & Master Latency Timer & Cache Line Size
Table 20. BIST & Header Type & Master Latency Timer & Cache Line Size

Field	Name	Description	Reset Value	R	W	I
31	BIST Capable	Unsupported	0	O	X	X
30	Start BIST	Unsupported	0	O	X	X
29:28	Reserved	Unsupported	00	O	X	X
27:24	BIST Completion Code	Unsupported	0000	O	X	X
23	Header Type	This bit identifies whether or not the device contains multiple functions.	0	O	X	X
22:16	Configuration Type	This 7bit code identifies the layout of the second part of the predefined header.	0000000	O	X	X
15:8	Master Latency	Unsupported	00000000	O	X	X
7:0	Cache Line Size	Unsupported	00000000	O	X	X

5.2.5. Base Address for I/O Mapped Mode Registers
Table 21. Base Address for I/O Mapped Mode Registers

Field	Name	Description	Reset Value	R	W	I
31:6	Base Address	Base Address for Mode Registers.	11111111 11111111 11111111 11	O	O	X
5:2	Base Address	Base Address for Mode Registers. These 4 bits are fixed at "0" because Mode Registers always need 64byte as address space.	0000	O	X	X
1	Reserved		0	O	X	X
0	I/O Access Indicator	This bit indicates accepting I/O access for Mode Registers	1	O	X	X

5.2.6. Base Address for Memory Mapped Mode Registers
Table 22. Base Address for Memory Mapped Mode Registers

Field	Name	Description	Reset Value	R	W	I
31:6	Base Address	Base Address for Mode Registers.	11111111 11111111 11111111 11	O	O	X
5:4	Base Address	Base Address for Mode Registers. These 2 bits are fixed at "0" because Mode Registers always need 64byte as address space.	00	O	X	X
3	Pre-fetch	Unsupported	0	O	X	X
2:1	Address Type	Unsupported	00	O	X	X
0	Memory Access Indicator	This bit indicates accepting memory access for Mode Registers	0	O	X	X

5.2.7. Base Address for I/O Mapped Local Bus Control
Table 23. Base Address for I/O Mapped Local Bus Control

Field	Name	Description	Reset Value	R	W	I
31:2	Base Address	Base Address for Local Bus Control. This register is used in conjunction with I/O Range Register of Mode Registers.	00000000 00000000 00000000 00000000	O	O	X
1	Reserved		0	O	X	X
0	I/O Access Indicator	This bit indicates accepting I/O access for Local Bus.	1	O	X	X

5.2.8. Base Address for Memory Mapped Local Bus Control
Table 24. Base Address for Memory Mapped Local Bus Control

Field	Name	Description	Reset Value	R	W	I
31:4	Base Address	Base Address for Local Bus Control. This register is used in conjunction with Memory Range Register of Mode Registers.	000000000 000000000 000000000 0000	O	O	X
3	Pre-fetch	Unsupported	0	O	X	X
2:1	Address Type	Unsupported	00	O	X	X
0	Unsupported Indicator	This bit indicates accepting memory access for Local Bus.	0	O	X	X

5.2.9. Cardbus CIS Pointer
Table 25. Cardbus CIS Pointer

Field	Name	Description	Reset Value	R	W	I
31:0	Card Bus CIS Pointer	Unsupported	00000000 00000000 00000000 00000000	O	X	X

5.2.10. Subsystem ID & Subsystem Vendor ID
Table 26. Subsystem ID & Subsystem Vendor ID

Field	Name	Description	Reset Value	R	W	I
31:16	Subsystem ID	This 16 bits code is used to identify the expansion board.	00000000 00000000	O	X	O
15:0	Subsystem Vendor ID	This 16 bits code is used to identify the vendor of the expansion board.	00000000 00000000	O	X	O

5.2.11. Expansion ROM Base Address
Table 27. Expansion ROM Base Address

Field	Name	Description	Reset Value	R	W	I
31:0	Expansion ROM Base Address	Unsupported	00000000 00000000 00000000 00000000	O	X	X

5.2.12. Capabilities Pointer
Table 28. Capabilities Pointer

Field	Name	Description	Reset Value	R	W	I
31:8	Reserved		00000000 00000000 00000000	O	X	X
7:2	Cap_Ptr	This register points to the first item in the list of capabilities.	010000	O	X	X
1:0	Reserved		00	O	X	X

5.2.13. Max_Lat & Min_Gnt & Interrupt Pin & Interrupt Line
Table 29. Max_Lat & Min_Gnt & Interrupt Pin & Interrupt Line

Field	Name	Description	Reset Value	R	W	I
31:24	Max_Lat	Unsupported	00000000	O	X	X
23:16	Min_Gnt	Unsupported	00000000	O	X	X
15:8	Interrupt Pin	This register tells which interrupt pin the device uses. ZEN7201AF uses INTA# only. If the interrupt pin is not needed, put "0" in this register.	00000001	O	X	O
7:0	Interrupt Line	This register is used to communicate interrupt line routing information.	00000000	O	O	X

5.2.14. HSCSR & Nxt_Ptr & Cap_ID
Table 30. HSCSR & Nxt_Ptr & Cap_ID

Field	Name	Description	Reset Value	R	W	I
31:24	Reserved		00000000	O	X	X
23	Insertion	This bit is set when the ejector handle is closed (i.e. when detecting the falling edge of MSW). This bit is cleared by writing "1" to its location.	0	O	O	X
22	Extraction	This bit is set when the ejector handle is unlocked (i.e. when detecting the rising edge of MSW). This bit is cleared by writing "1" to its location.	0	O	O	X
21:20	Reserved		00	O	X	X
19	LED On/Off	This bit controls an external LED indicator for user feedback. When software writes "1" to this register, LEDO# outputs Low. But when reset is asserted, LEDO# is asserted in dependent of the state of this bit.	0	O	O	X
18	Reserved		0	O	X	X
17	ENUM# Mask	This bit allows the ENUM# pin to be masked by software. Writing "1" to this bit masks the ENUM# pin from being driven. Writing "0" to this bit will enable ENUM# to be driven. ENUM# state itself is a result of the INS and EXT bits.	0	O	O	X
16	Reserved		0	O	X	X
15:8	NXT_PTR	Pointer to the next item in the capabilities list. ZEN7201AF has no more item, so this register is always 00h.	00000000	O	X	X
7:0	Cap_ID	This register is 06h because ZEN7201AF supports "Hot Swap".	00000110	O	X	X

5.3. Mode Registers

Table 31 - 37 show the details of Mode Registers.

5.3.1. Range Register for I/O Access

Table 31. Range Register for I/O Access

Field	Name	Description	Reset Value	R	W	I
31:16	Reserved		11111111 11111111	O	X	X
15:2	Local Range for I/O	This register specifies the range of PCI address to be recognized as an access to ZEN7201AF. Each bits corresponds to an address bit. A value of "1" indicates this bit is to be included in decode. This register is used in conjunction with Base Address for I/O Mapped Local Bus Control (18h).	11111111 110000	O	X	O
1	Reserved		0	O	X	X
0	I/O Access Indicator	This bit indicates accepting I/O access for Local Bus.	1	O	X	X

5.3.2. Bank Register for I/O Access

Table 32. Bank Register for I/O Access

Field	Name	Description	Reset Value	R	W	I
31:16	Reserved		00000000 00000000	O	X	X
15:2	Bank Address for I/O	The value of this register and PCI address are synthesized and outputted to local address bus. About the details, please refer to 4.2.3. Local Bus Addressing.	00000000 000000	O	O	O
1:0	Reserved		00	O	X	X

5.3.3. Range Register for Memory Access
Table 33. Range Register for Memory Access

Field	Name	Description	Reset Value	R	W	I
31:24	Reserved		11111111	O	X	X
23:4	Local Range for I/O	This register specifies the range of PCI address to be recognized as an access to ZEN7201AF. Each bit corresponds to an address bit. A value of "1" indicates this bit is to be included in decode. This register is used in conjunction with Base Address for Memory Mapped Local Bus Control (1Ch).	11110000 00000000 0000	O	X	O
3:1	Reserved		000	O	X	X
0	Memroy Access Indicator	This bit indicates accepting I/O access for Local Bus.	0	O	X	X

5.3.4. Bank Register for Memory Access
Table 34. Bank Register for Memory Access

Field	Name	Description	Reset Value	R	W	I
31:24	Reserved		00000000	O	X	X
23:4	Bank Address for I/O	The value of this register and PCI address are synthesized and outputted to local address bus. About the details, please refer to 4.2.3. Local Bus Addressing.	00000000 00000000 0000	O	O	O
3:0	Reserved		0000	O	X	X

5.3.5. Timing Control Register

Table 35. Timing Control Register

Field	Name	Description	Reset Value	R	W	I
31:28	Reserved		0000	0	X	X
27	I/O Chip Select Enable	When this bit is set "1", the built-in address decoder can be used.	0	0	0	0
26:24	I/O Chip Select Decode	These bits specify what bit positions are used to decode PCI address for chip select.	000	0	0	0
23:20	Memory Access Address Hold	These bits specify number of local bus cycles from deasserting MEW#/MER# to deasserting LADR. Number of clocks is the value of this register plus 3.	0000	0	0	0
19:16	Memory Access Pulse Width	These bits specify number of local bus cycles from asserting MEW#/MER# to deasserting it. Number of clocks is the value of this register plus 2. When WAIT# is enabled, this function is not valid (i.e. the pulse width of MEW#/MER# is depending on WAIT#).	0000	0	0	0
15:12	Memory Access Address Setup	These bits specify number of local bus cycles from asserting LADR to asserting MEW#/MER#. Number of clocks is the value of this register plus 2.	0000	0	0	0
11:8	I/O Access Address Hold	These bits specify number of local bus cycles from deasserting IOW#/IOR# to deasserting LADR. Number of clocks is the value of this register plus 3.	0000	0	0	0
7:4	I/O Access Pulse Width	These bits specify number of local bus cycles from asserting IOW#/IOR# to deasserting it. Number of clocks is the value of this register plus 2. When WAIT# is enabled, this function is not valid (i.e. the pulse width of IOW#/IOR# is depending on WAIT#).	0000	0	0	0
3:0	I/O Access Address Setup	These bits specify number of local bus cycles from asserting LADR to asserting IOW#/IOR#. Number of clocks is the value of this register plus 2.	0000	0	0	0

5.3.6. EEPROM Control Register

Table 36. EEPROM Control Register

Field	Name	Description	Reset Value	R	W	I
31:8	Reserved		00000000 00000000 00000000	0	X	X
7:5	Reserved		000	0	X	X
4	EEPROM Monitor	The value of the pin EEN can be read via this bit.	X	0	X	X
3	EEPROM Data Out	The value of this bit is outputted to EDO.	0	0	0	X
2	EEPROM Data In	The value of the pin EDI can be read via this bit.	X	0	X	X
1	EEPROM Chip Select	The value of this bit is outputted to ECS.	0	0	0	X
0	EEPROM Clock	The value of this bit is outputted to ESK.	0	0	0	X

5.3.7. Device Control & Interrupt Control Register
Table 37. Device Control & Interrupt Control Register

Field	Name	Description	Reset Value	R	W	I															
31:24	USERDEF	The free area for identifying the board with ZEN7201AF.	00000000	O	X	O															
23:19	Reserved		00000	O	X	X															
18	Bus Width Select	This bit specify the width of the local data bus. When LDAT is used as 8 bit bus, this bit should be set "0". When LDAT is used as 16 bit bus, this bit should be set "1".	0	O	O	O															
17	WAIT# Enable Select	Enabling the pin WAIT# when this bit is set "1".	0	O	O	O															
16	Local Reset	Asserting LRST# while this bit is set "0".	1	O	O	X															
15:6	Reserved		00000000 00	O	X	X															
5	IRQ Monitor	The value of the pin IRQ can be read via this bit.	X	O	X	X															
4	Interrupt Reset	Writing "1" to this bit resets INTA#.	0	X	O	X															
3	Interrupt Monitor	The status of INTA# can be read via this bit.	1	O	X	X															
2:1	Interrupt Condition	<p>These bits specify the condition of IRQ for generating PCI Interrupt. This condition should be set before Interrupt Enable (bit [0]) and once the condition is set, don't change again. It takes 4 local clocks for this condition to be valid after writing this register.</p> <p>The following table shows the condition for generating PCI Interrupt.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>bit[2]</th> <th>bit[1]</th> <th>Condition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 for 2clk</td> </tr> <tr> <td>0</td> <td>1</td> <td>Rising edge</td> </tr> <tr> <td>1</td> <td>0</td> <td>Falling edge</td> </tr> <tr> <td>1</td> <td>1</td> <td>1 for 2clk</td> </tr> </tbody> </table>	bit[2]	bit[1]	Condition	0	0	0 for 2clk	0	1	Rising edge	1	0	Falling edge	1	1	1 for 2clk	00	O	O	O
bit[2]	bit[1]	Condition																			
0	0	0 for 2clk																			
0	1	Rising edge																			
1	0	Falling edge																			
1	1	1 for 2clk																			
0	Interrupt Enable	Enabling PCI Interrupt when this bit is set "1".	0	O	O	X															

6. Timing Diagrams

6.1. Local I/O Access

The timing of I/O Access depends on the setting of Timing Control Register.

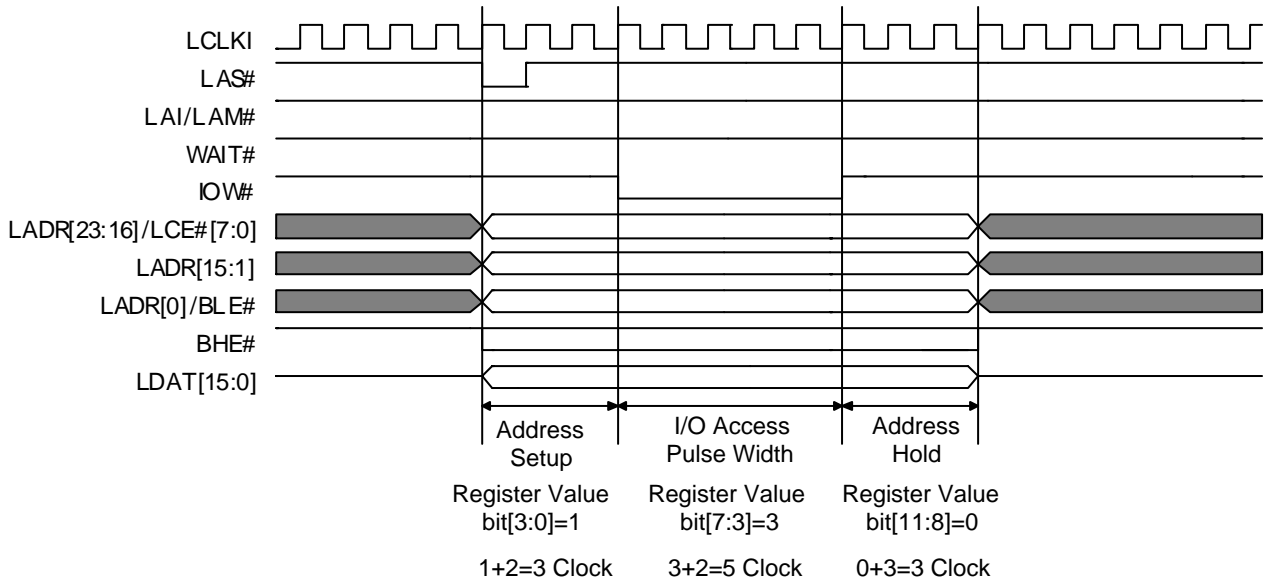


Fig.18 I/O Write Access

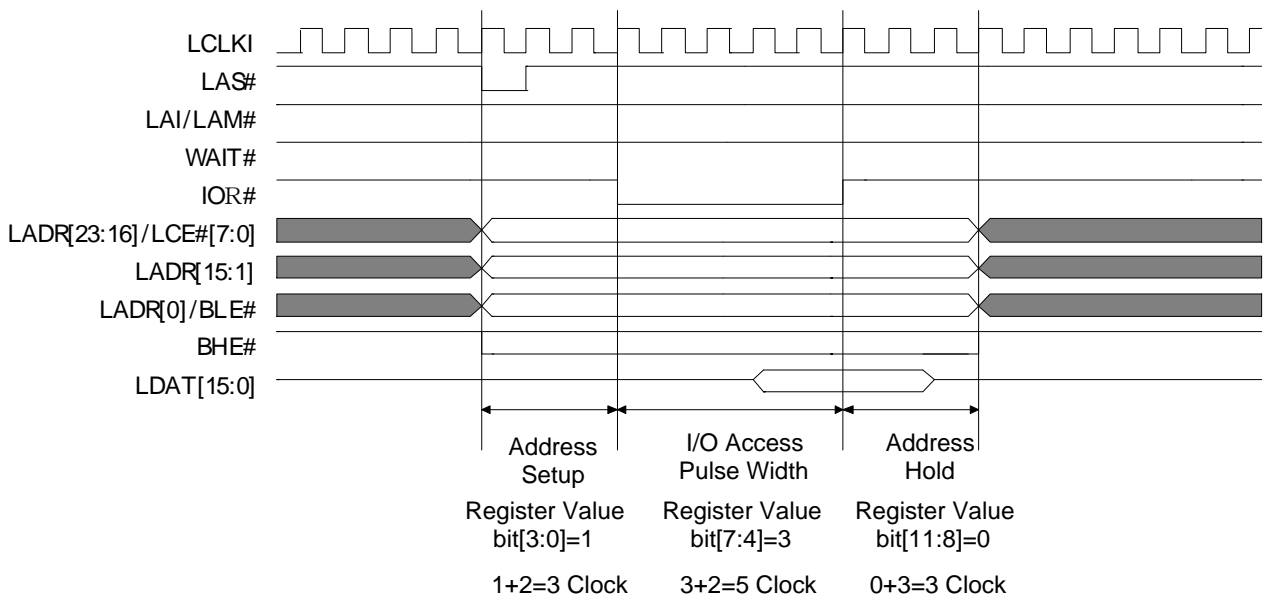


Fig.19 I/O Read Access

6.2. Local Memory Access

The timing of Memory Access depends on the setting of Timing Control Register.

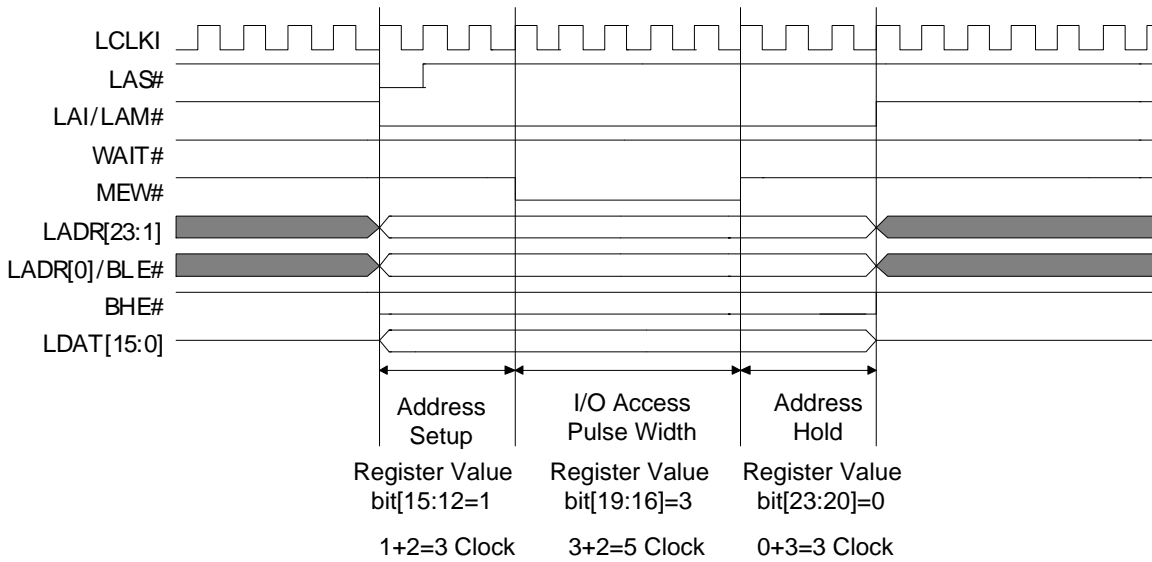


Fig.20 Local Memory Write Access

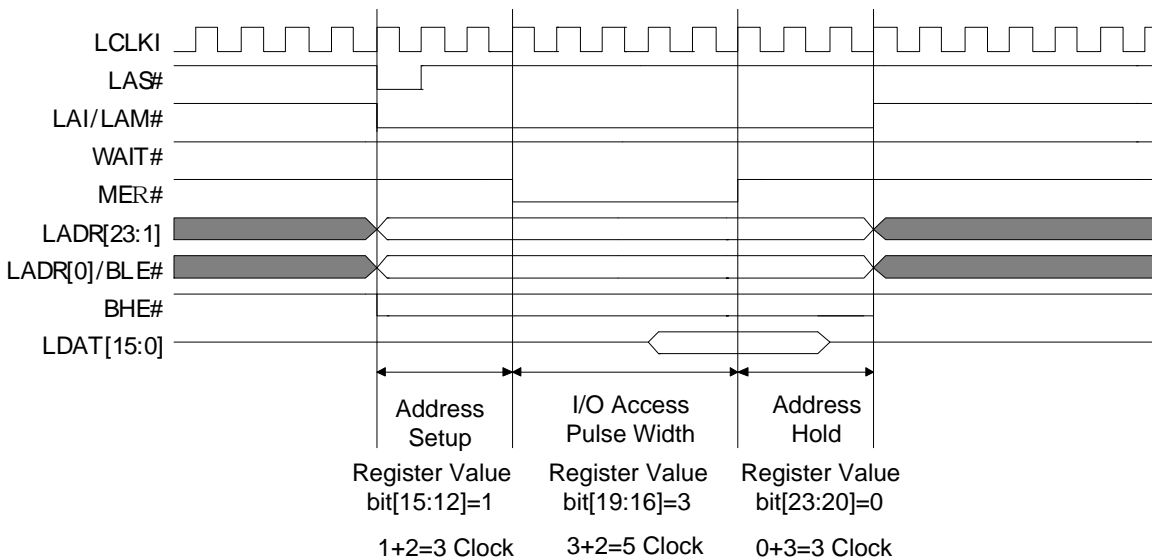


Fig.21 Local Memory Read Access

6.3. Wait Access

6.3.1. Local I/O Access

In the case of enabling WAIT#, the setting of I/O Access Pulse Width is ignored.

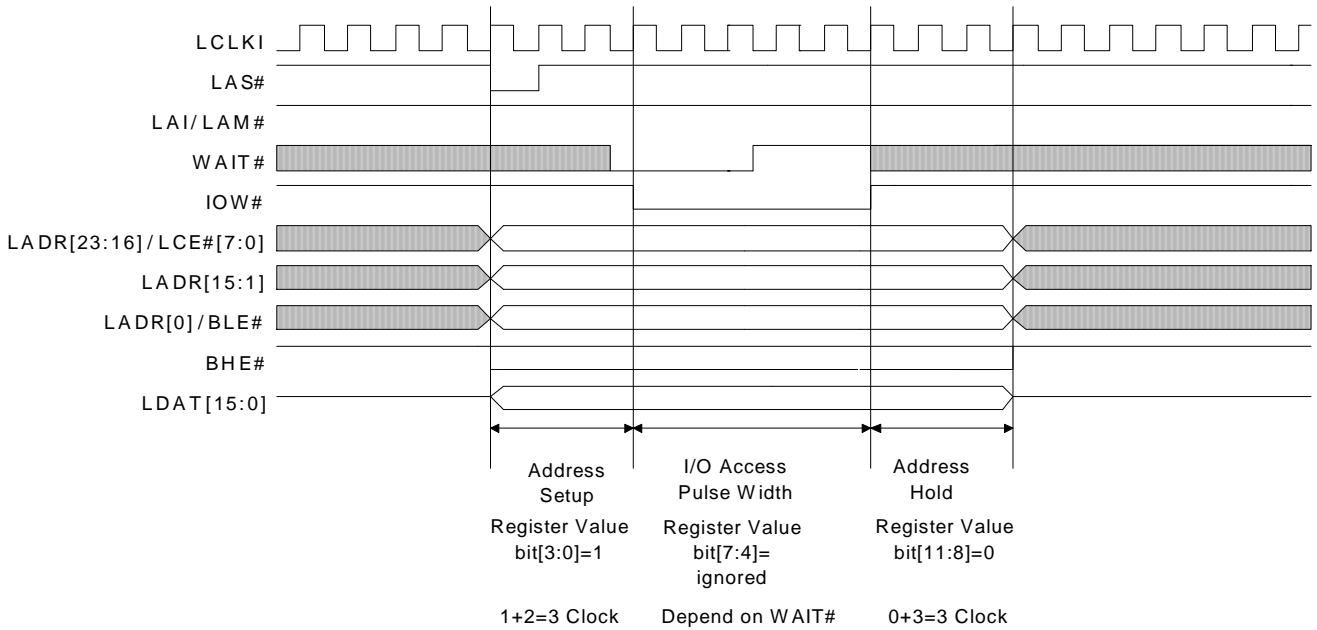


Fig.22 I/O Write Access (With WAIT#)

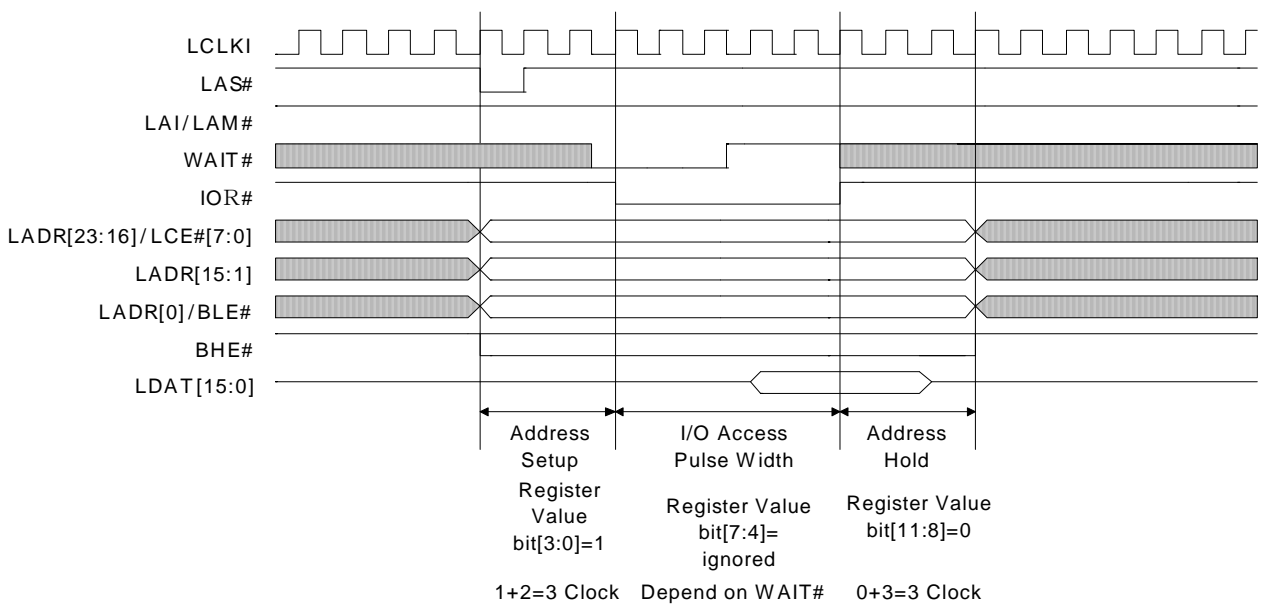


Fig.23 I/O Read Access (With WAIT#)

6.3.2. Local Memory Access

In the case of enabling WAIT#, the setting of Memory Access Pulse Width is ignored.

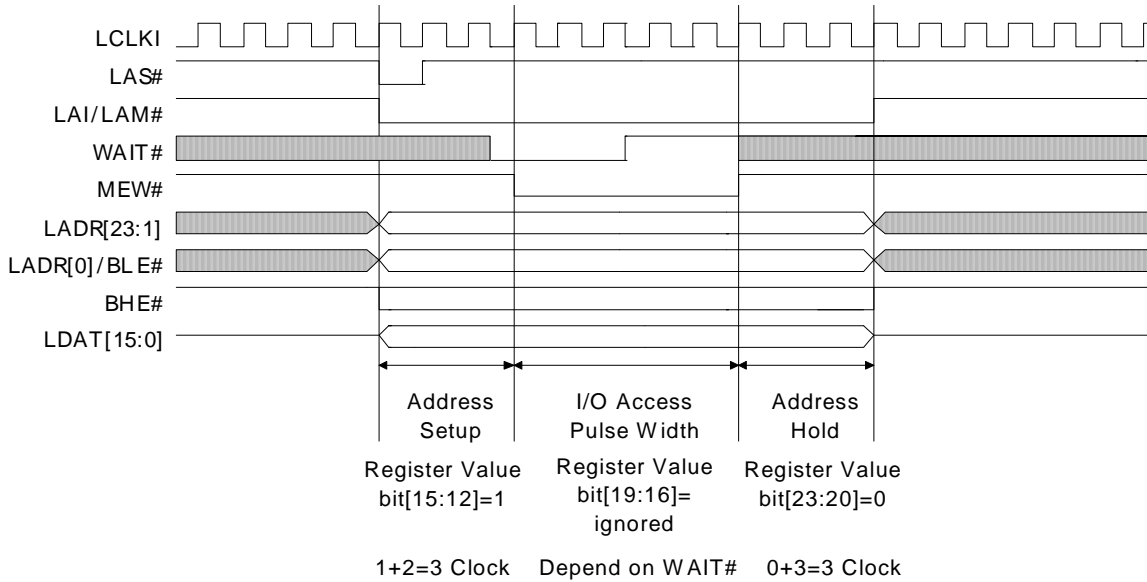


Fig.24 Memory Write Access (With WAIT#)

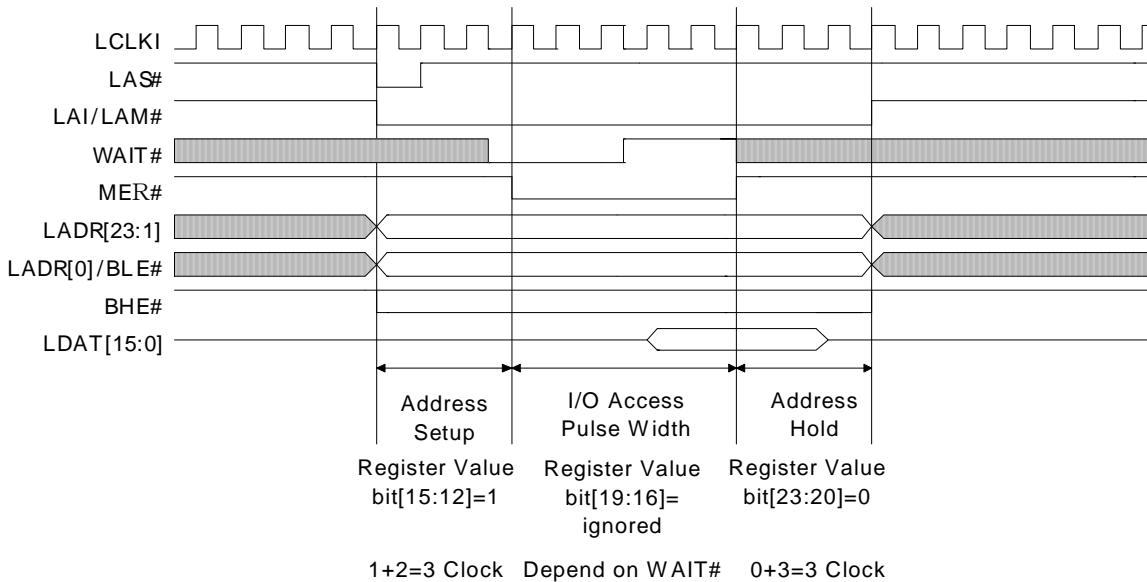


Fig.25 Memory Read Access (With WAIT#)

6.4. Interrupt

Once IRQ meets the condition of generating PCI Interrupt, INTA# is asserted. Figure 26 shows the timing diagram for example.

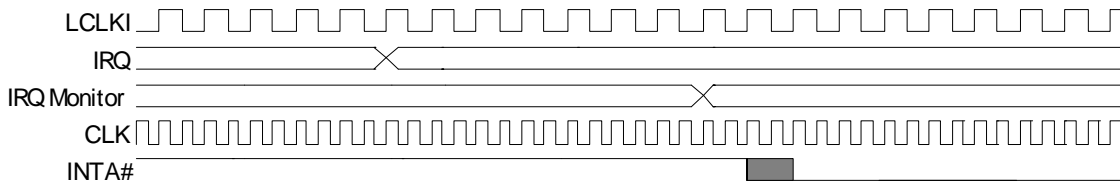


Fig.26 Interrupt Cycle

7. Electrical Specifications

7.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{dd}	-0.3 to +7.0	V
Input voltage	V _{in}	-0.3 to V _{DD} +0.3	V
Output voltage	V _{out}	-0.3 to V _{DD} +0.3	V
Input current	I _{in}	-10 to +10	mA
Storage temperature	T _{stg}	-40 to +125	°C

7.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{dd}	4.75	5.00	5.25	V
Operation temperature	T _{opr}	0	-	+70	°C

7.3. DC Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Input "High" voltage	V _{ih}		2.2		V
Input "Low" voltage	V _{il}			0.8	V
Input "High" current	I _{ih}	V _{in} =V _{dd}	-10	10	uA
Input "Low" current	I _{il}	V _{in} =V _{ss}	-10	10	uA
Output "High" voltage	V _{oh}	I _{oh} =-4mA	2.4		V
Output "Low" voltage	V _{ol}	I _{ol} =4mA		0.4	V
Standby current	I _{dds}	V _{in} =V _{dd} or V _{ss}		17	uA
Operation current	I _{ddo}			60	mA

Note) Applied to the pins except PCI bus signals. As to them, please refer to PCI Specification. I_{oh} is Output "High" current and I_{ol} is Output "Low" current.

7.4. AC Characteristics

Table 41. AC Characteristics

Parameter	Signal	Symbol	Min	Typ	Max	Unit
IRQ setup time	IRQ	TIRQS	10			ns
IRQ hold time	IRQ	TIRQH	10			ns
WAIT# setup time	WAIT#	TWAITS	10			ns
WAIT# hold time	WAIT#	TWAITH	0			ns
Local clock input high pulse width	LCLKI	TLCIH	12.50			ns
Local clock input low pulse width	LCLKI	TLCIL	12.50			ns
Local clock input cycle time	LCLKI	TLCICY		30		ns
Local clock output delay time	LCLKO	TLCOD	0		5	ns
Local clock output high pulse width	LCLKO	TLCOH	25		35	ns
Local clock output low pulse width	LCLKO	TLCOL	25		35	ns
Local clock output cycle time	LCLKO	TLCOCY		60		ns
Local address delay time	LADR	TLAD	0		5	ns
Local data setup time	LDAT	TLDS	10			ns
Local data hold time	LDAT	TLDH	0			ns
Local data delay time	LDAT	TLDD	0		5	ns
Local control signal delay time	LAS#, LAI/LAM#	TLCD	0		5	ns
Local read strobe delay time	MER#, IOR#	TLRD	0		5	ns
Local write strobe delay time	MEW#, IOW#	TLWD	0		5	ns
ESK high pulse width	ESK	TESKH	1.89		1.95	us
ESK low pulse width	ESK	TESKL	1.89		1.95	us
ESK cycle time	ESK	TESKCY		3.84		us
ESK delay time	ESK	TECD	0		30	ns
ESK start from asserting ECS	ESK ECS	TESKRU	1.83		2.79	us
Deasserting ECS from ESK stop	ESK ECS	TESKFD	1.89		4.95	us
ECS delay time	ECS	TECSD	0		30	ns
ECS interval time	ECS	TECSRU	9.57		9.63	us
EDI setup time	EDI	TEDIS	30			ns
EDI hold time	EDI	TEDIH	0			ns
EDO valid from asserting ECS	EDO	TEDOD0	0.96		1.02	us
EDO delay time from ESK	EDO	TEDOD1	2.94		3.00	us

Note) All characteristics at PCI clock 33MHz.

Local address includes LADR [23:0] and BHE#.

7.5. Timing Diagram

7.5.1. Local Access Timing Diagram

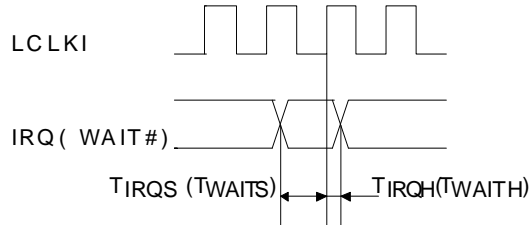
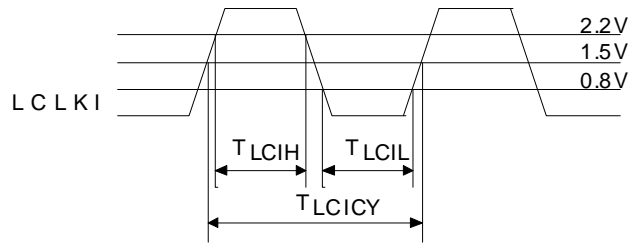
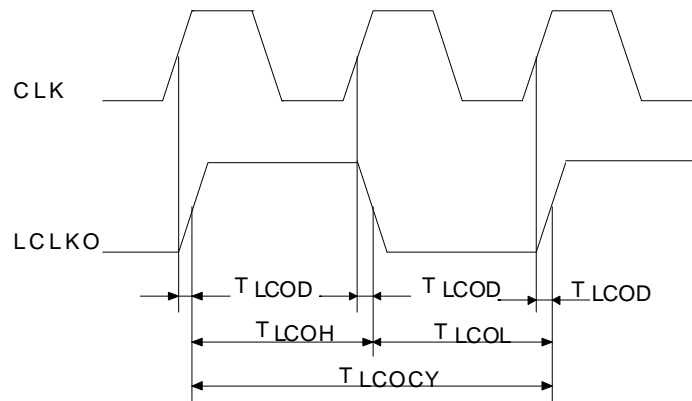


Fig.27 Local Input Signal Setup and Hold Timing

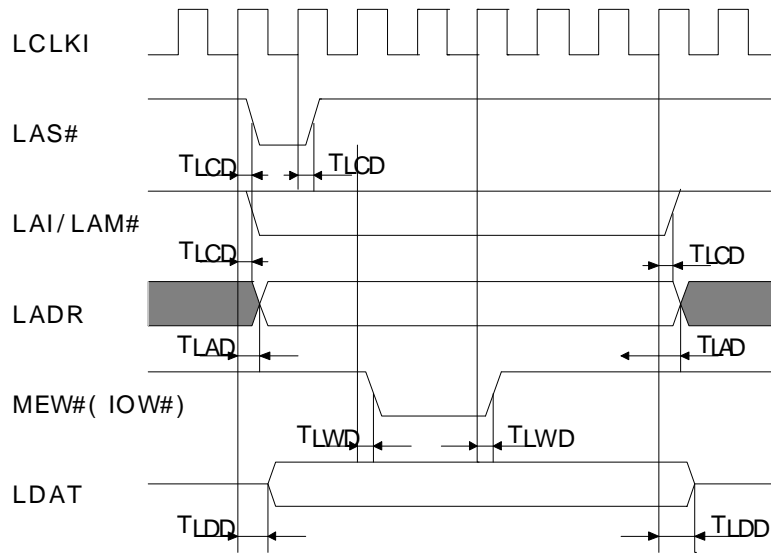


(a). LCLKI Timing

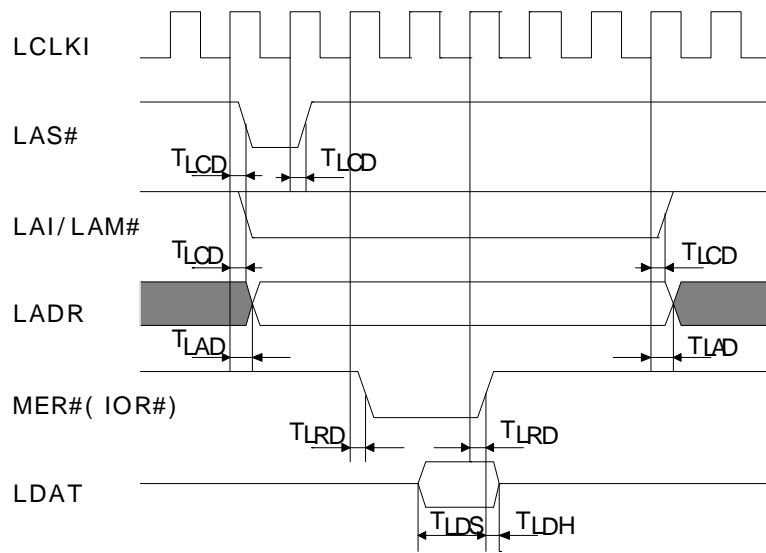


(b). LCLKO Timing

Fig.28 Local Clock Timing



(a). Write Cycle



(b). Read Cycle

Fig.29 Local I/O Signal Setup, Hold and Delay Timing

7.5.2. EEPROM Access Diagram

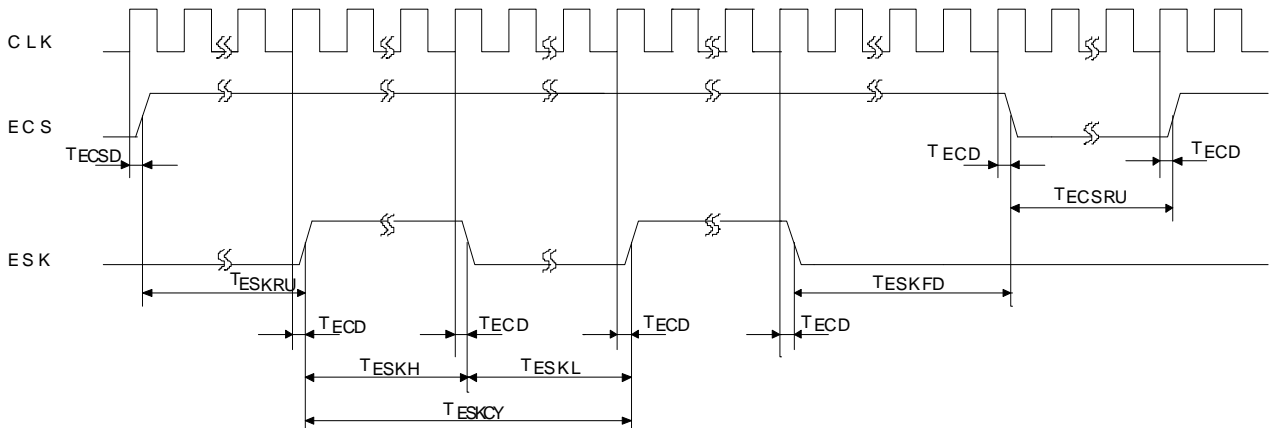


Fig.30 ESK, ECS Timing

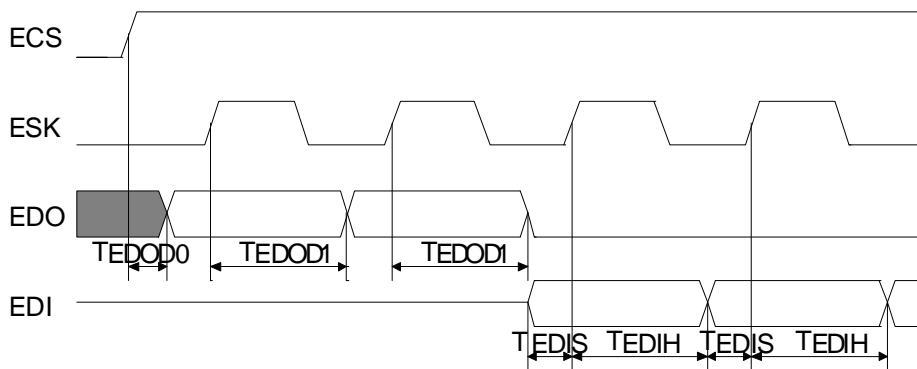


Fig.31 EDO, EDI Timing

8. Package Outline

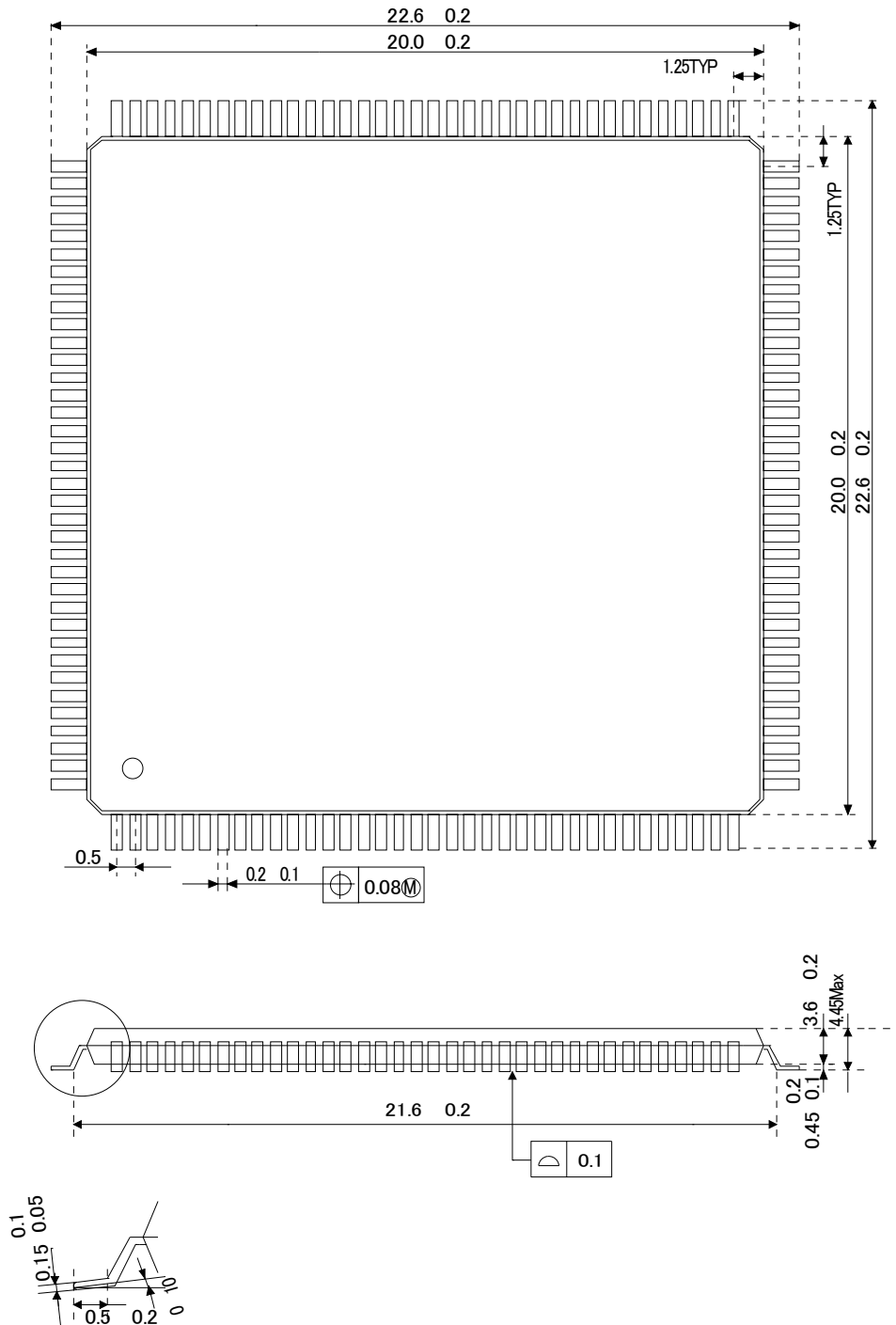


Fig.32 Outline Dimensions

9. Note

1. Don't keep an unused input terminal open.
2. Please add outer pull up or down to LDAT[15:0] because they do not have an internal pull up.

10.Revision History

Version	Date	Contents
1.0	2002/3/1	First edition issue
1.1	2009/3/11	Company address changed

Note

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